REMARKS

The Applicants appreciate the Examiner's thorough examination of the subject application. Applicants request reconsideration of the subject application based on the following amendments and remarks.

Claims 1-39 are currently pending in the application. Claims 1, 4, 7, 14, 22, and 27-30 have been amended and new claims 31-39 have been added. Support for the amendments may be found throughout the specification. No new matter has been added by the amendments to the specification or the claims. Support for claims 1, 7, 10, 14, 17, and 22 may be found at page 12, line 19 to page 13, line24. Support for new claims 27-30 may be found in Figure 1 and page 17, lines 9-23.

Claim 4 was rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject which applicant regards as the invention.

Applicants believe that claim 4, as amended, is fully compliant with all of the requirements of 35 U.S.C. §112 including the antecedant basis requirement of §112, second paragraph.

A brief description of the present invention may be of assistance in addressing the rejections set forth by the Examiner under §102 and §103.

The present invention provides an active matrix substrate, comprising:

electrode wires constituted by scanning electrode wiring and signal electrode wiring that are arranged in a lattice;

an insulating film provided at least on the electrode wires so as to have openings in predetermined areas at least on either the scanning electrode wiring or on the signal electrode wiring; and

a metal layer selectively stacked only on the electrode wiring in the openings.

That is, claims 1, 7, 14, and 22, as amended, provide active matrix substrates in which a metal layer (**12**) is selectively stacked on the electrode wiring, e.g., scanning electrode wiring (**2**) and signal electrode wiring (**6**), in holes of the insulating film (**8**). Thus, looking at Figure 2(e), the metal layer (**12**) is situated within the hole of the insulating film (**8**) and is in direct contact with signal electrode wiring (**6**).

Applicants have surprisingly discovered that resistance in the electrode wiring may be reduced by stacking the metal layer selectively on the electrode wiring within the hole in the insulting layer.

Claims 1, 5, 7, 11, 12, 22, 23, and 27-29 were rejected under 35 U.S.C. §102(e) as being allegedly anticipated by Kawahata et al. (U.S. Patent 6,356,318). The rejection is traversed.

Claims 2-4, 6, 8-10, 13-21, 24-26, and 20 were rejected under 35 U.S.C. §103(a) as being allegedly unpatentable over Kawahata as applied to claims 1, 5, 7, 11, 12, 22, 23, and 27-29.

For the sake of brevity, the two § 102 and § 103 rejections are addressed in combination. Such a combined response is considered appropriate because *inter alia* each of the rejections relies on the Kawahata patent as the sole or primary citation.

Each of the rejections is traversed.

The Office Action relies on the assertion that metal layer (15) is stacked on the electrode wiring in the opening (9) as the basis for the rejection of the claims under §102 and §103.

This assertion does not appear to be correct.

Kawahata teaches that an insulating layer (10) is deposited onto the gate insulation layer (8) prior to metal layer (15) deposition. Thus, Kawahata teaches at column 4, lines 50-55, that:

> The insulating film (10) is sandwiched between the gate line (7'), i.e., the lower electrode, and the upper electrode (15). The upper electrode is formed only in a flat region of the insulating film (10) and hence dielectric breakdown at steps in the insulating firm (10) does not occur easily.

It appears from the specification and Figures 1, 3, and 5 of Kawahata, that the reference fails to teach or suggest any active matrix substrate structure in which a metal layer (such as 15) is stacked on an electrode in a hole of an insulating layer.

As the reference is understood, all of structures recited by Kawahata comprise a metal layer deposited onto an insulator layer which is itself deposited on the electrode. More particularly, Kawahata teaches the deposition of a metal layer onto a relatively flat area of an insulating layer such that the insulating layer is interposed between metal layer and the electrode.

Thus, Kawahata neither discloses nor suggests the subject matter of claims 1, 7, 14 or 22. Therefore, for at least the reasons discussed *supra*, claims 1, 7, 14, and 22 are patentable over the teaching of Kawahata. Claims 2-6, 8-13, 15-21, and 23-26 and new claims 35-39 depend from one of claims 1, 7, 14, or 22 and are therefore also patentable over Kawahata.

Claims 27-30, which have been rewritten in independent format, correspond to claims 1, 7, 14, or 22 having the additional language "the opening and the metal layer are provided along substantially the whole length of at least either one of the scanning electrode wiring and the signal electrode wiring." Thus, Claims 27-30 are patentable over Kawahata, in part because Kawahata neither disclsoes nor suggests the subject matter of claims 27-30. Claims 31-34 depend from one of claims 27-30 and are therefore also patentable over Kawahata.

Although it is not believed that any additional fees are needed to consider this submission, the Examiner is hereby authorized to charge our deposit account no. 04-1105 should any fee be deemed necessary.

Respectfully submitted,

Date: May 16, 2003

John B. Alexander (Reg. No. 48,399)
EDWARDS & ANGELL, LLP
Dike, Bronstein, Roberts & Cushman
Intellectual Property Practice Group
P. O. Box 9169
Boston, MA 02209
Tel: (617) 439-4444
Fax: (617) 439-4170 / 7748

333130